

FIG 1

112

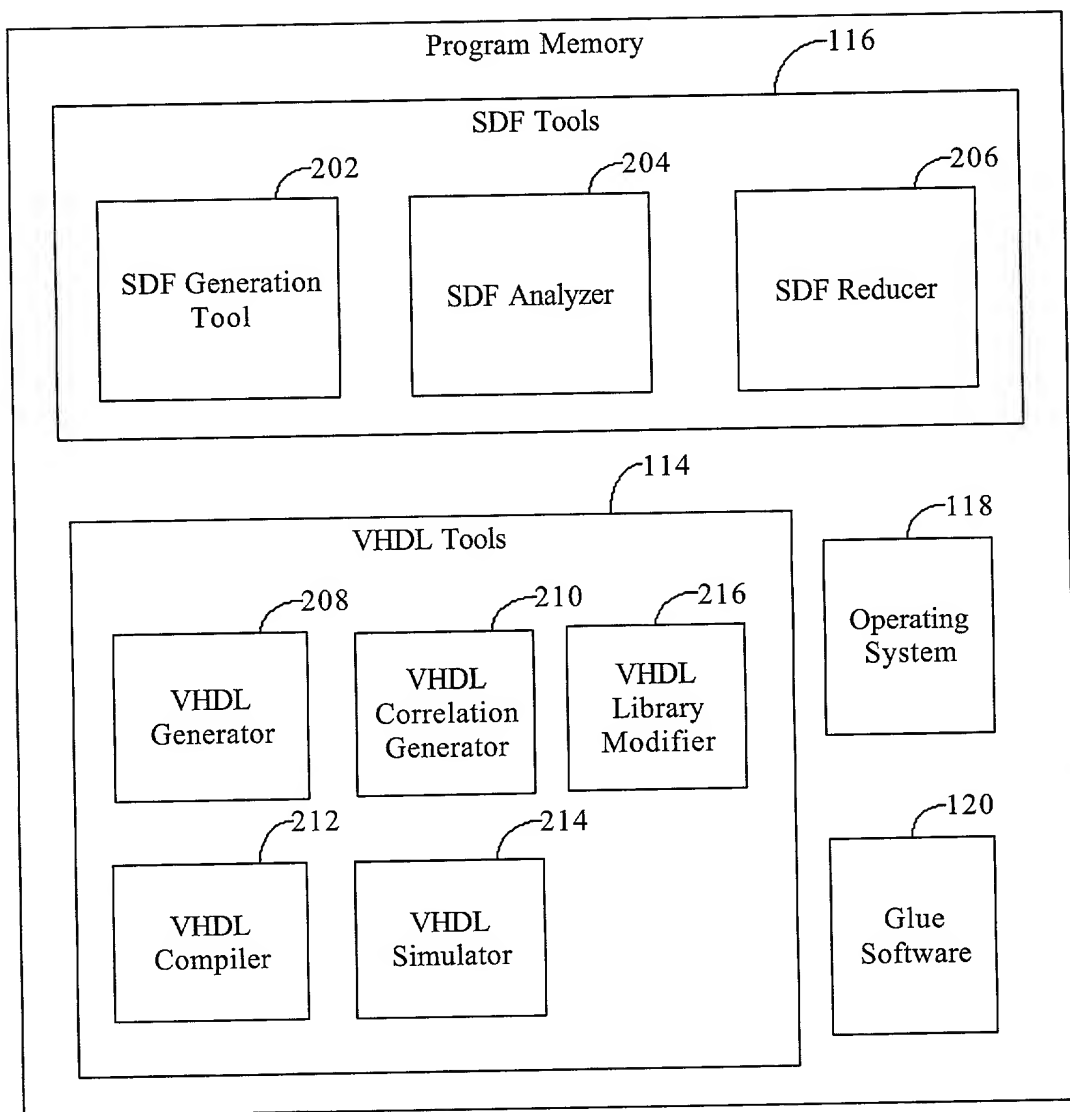


FIG 2

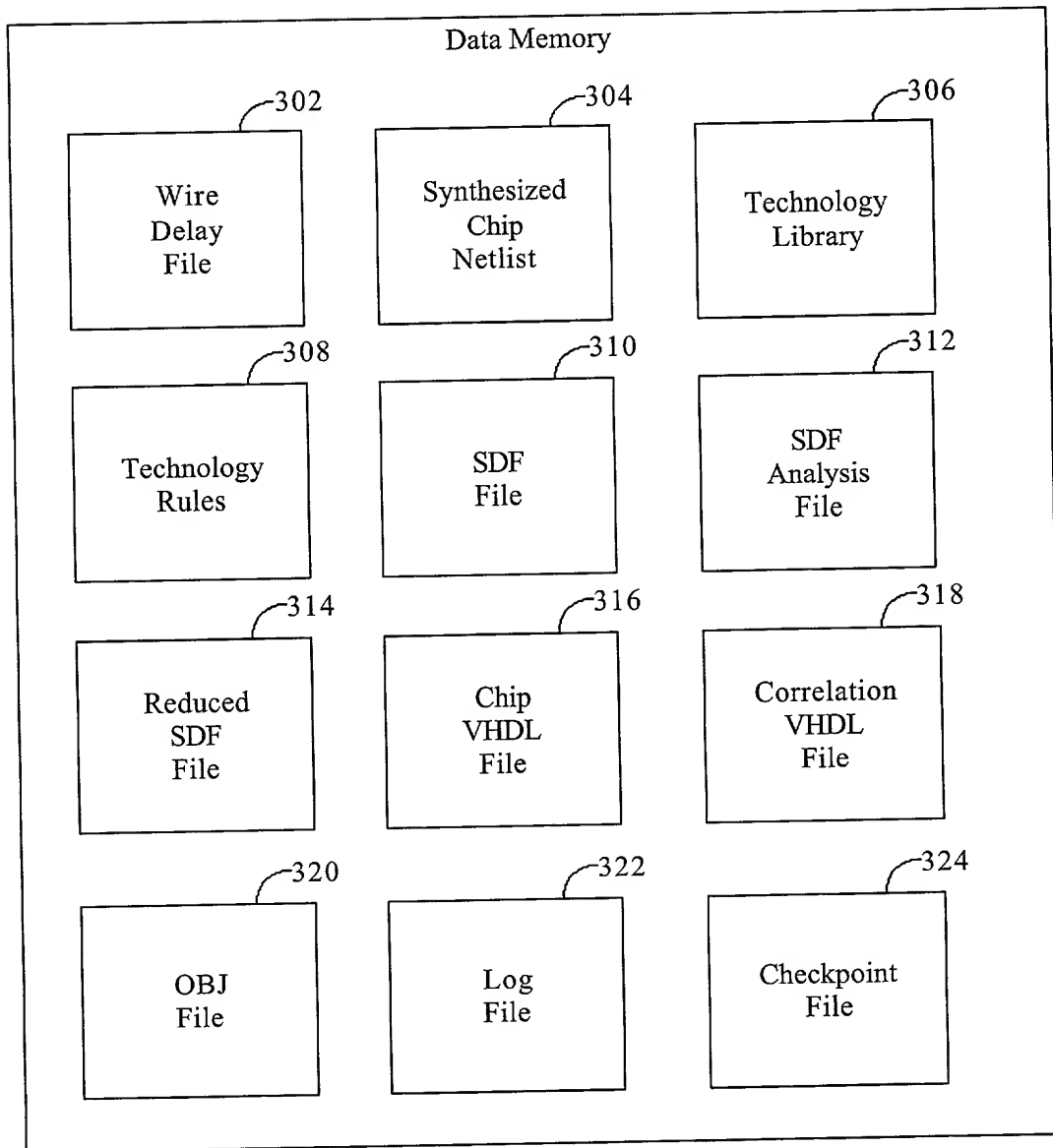
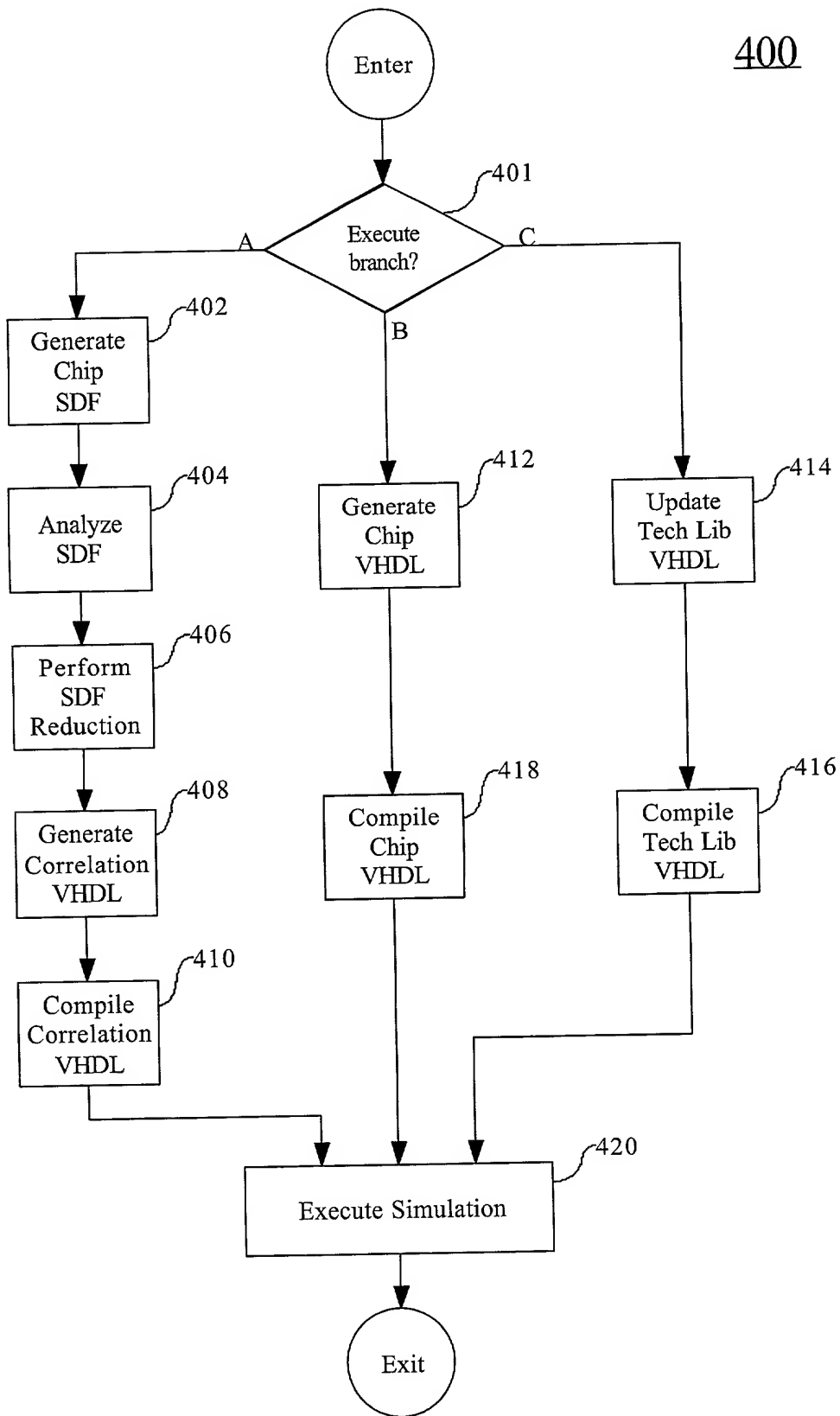


FIG 3

400



*FIG 4*

402

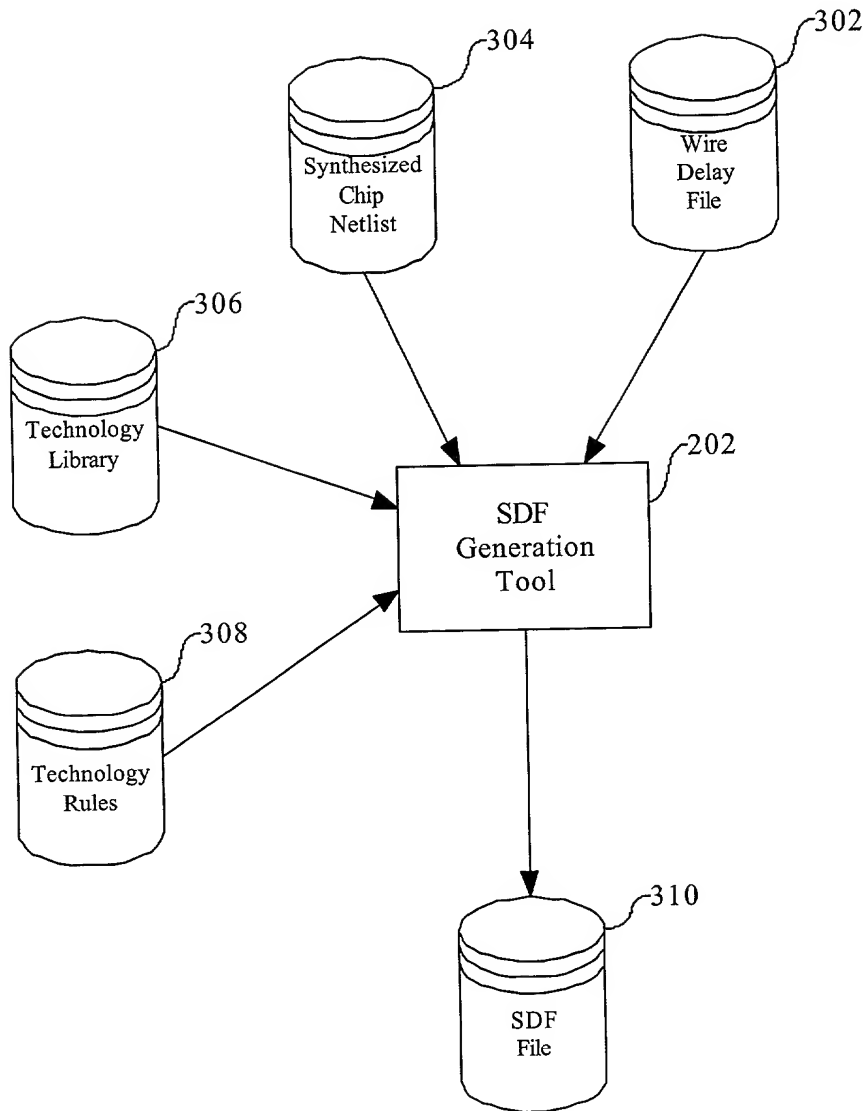


FIG 5

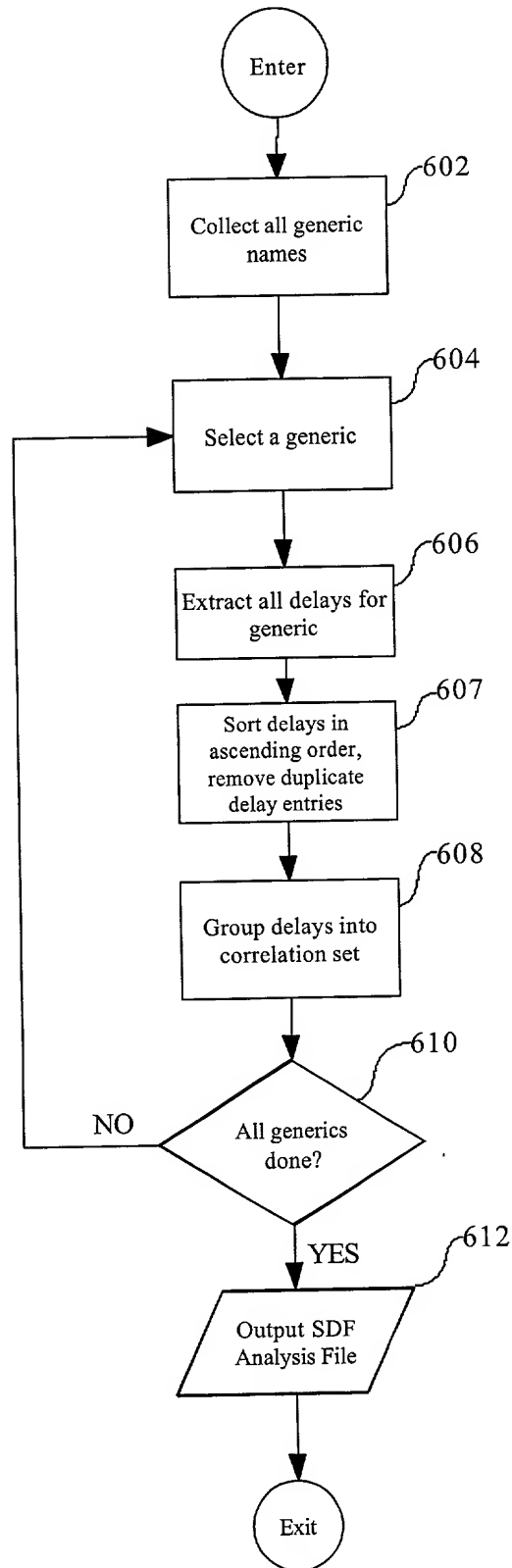


FIG 6

700

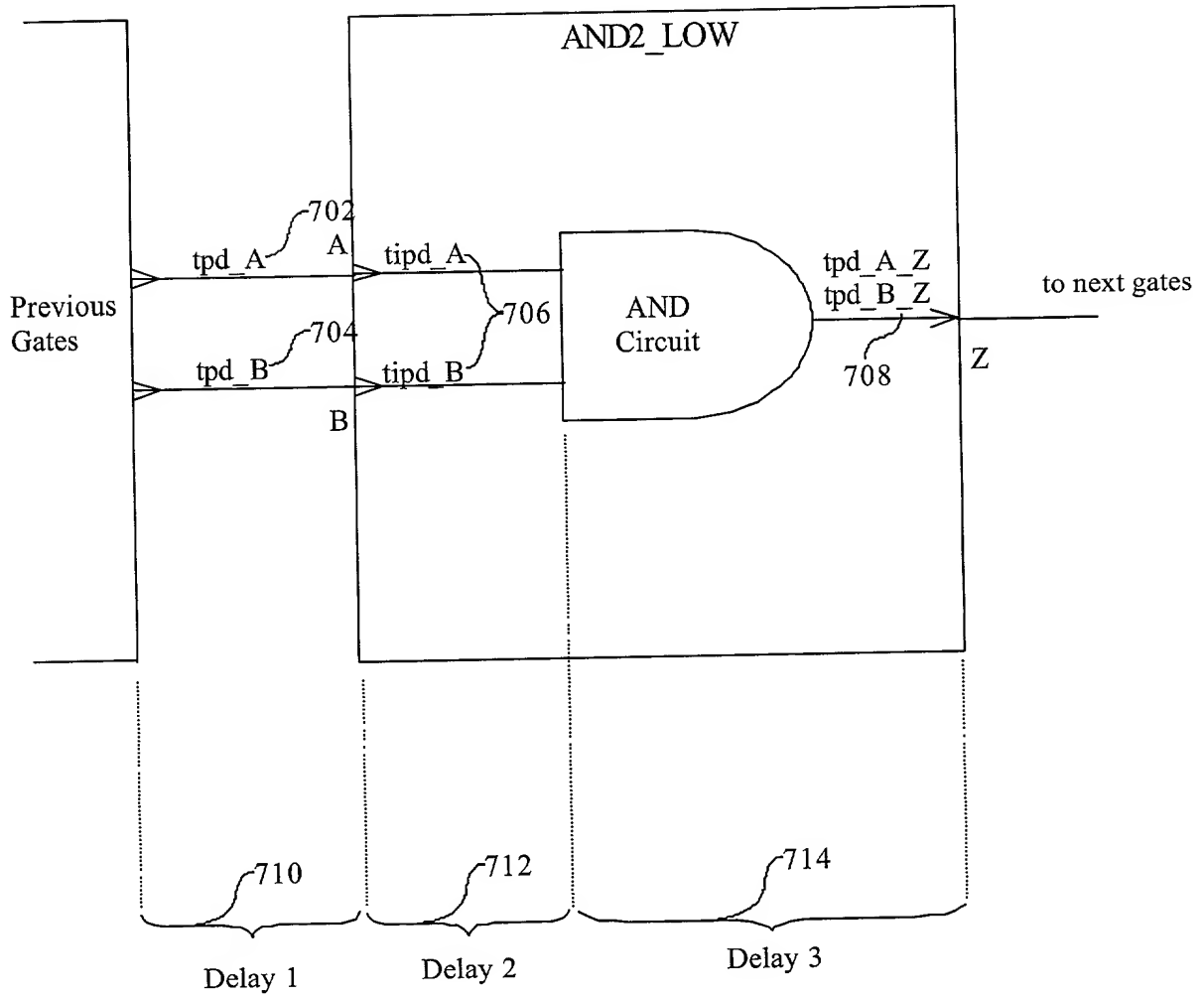
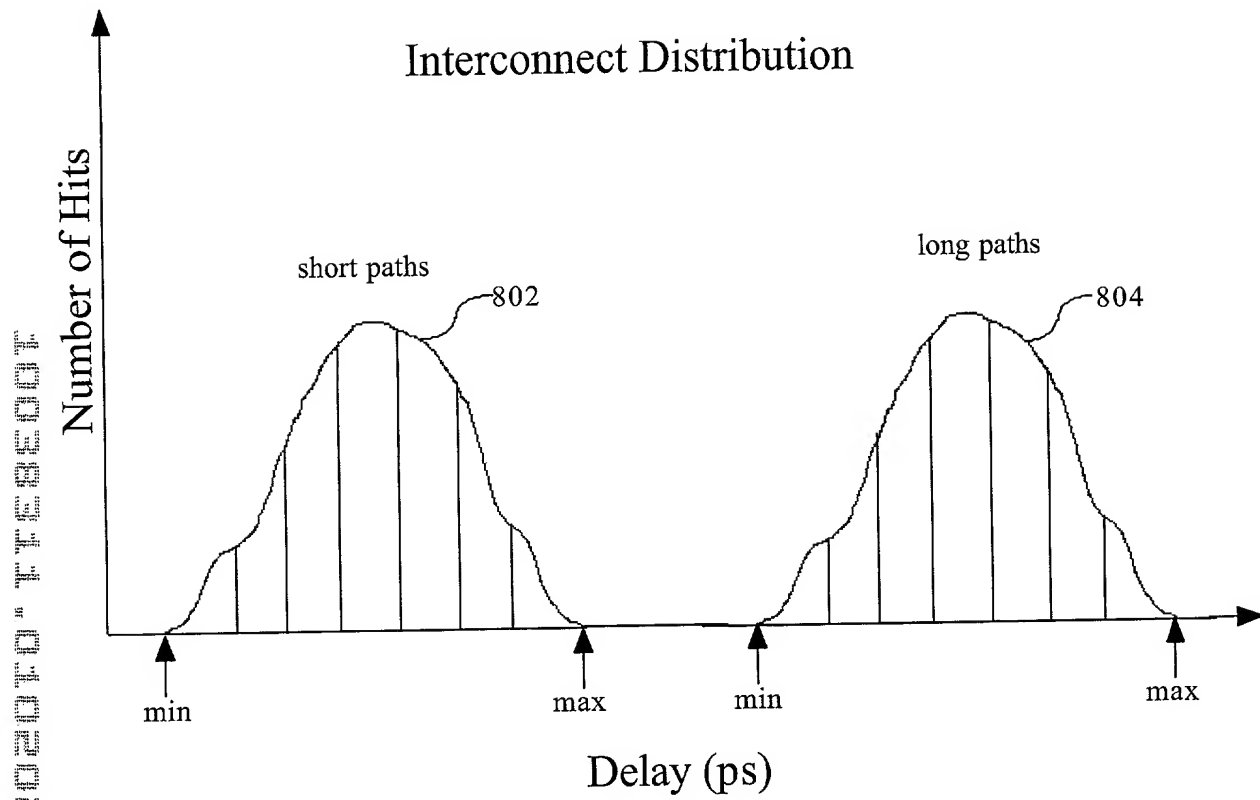


FIG 7

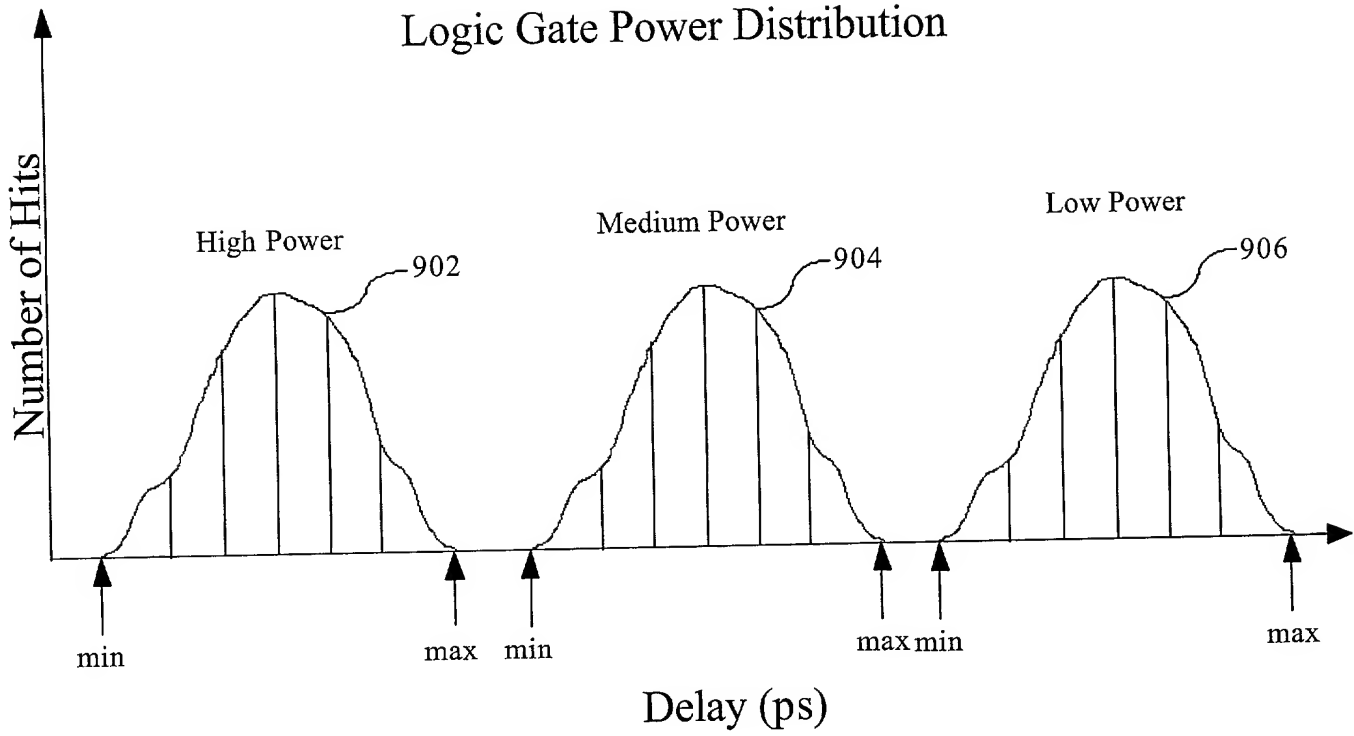
800



*FIG 8*

900

### Logic Gate Power Distribution



*FIG 9*

1000

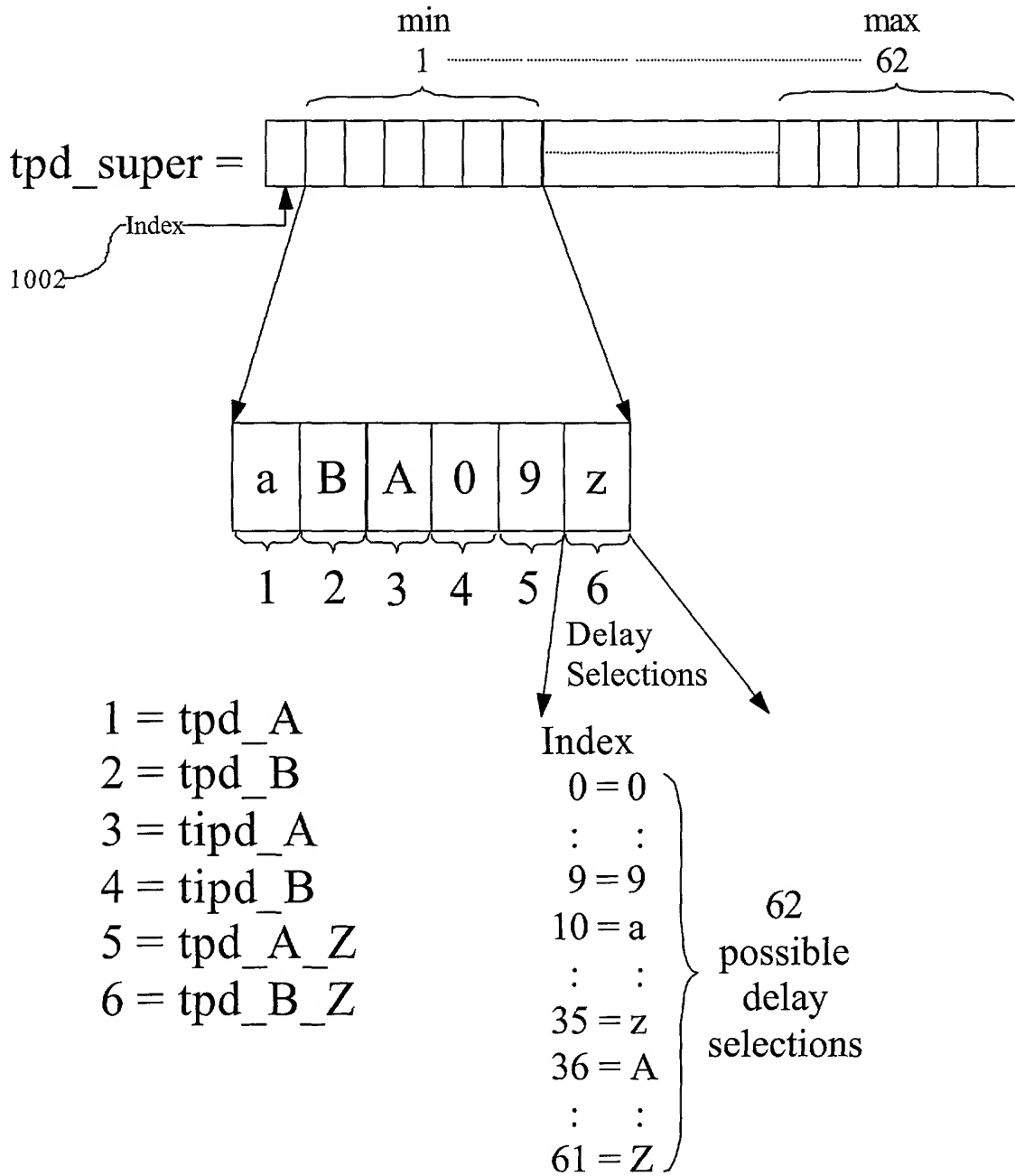


FIG 10

1100

Correlation Table

| BOOK_TYPE | MAPS TO  | SET SIZE |
|-----------|----------|----------|
| •         |          |          |
| •         |          |          |
| •         |          |          |
| AND2_MED  | AND2_NEW | 6        |
| •         |          |          |
| •         |          |          |
| •         |          |          |

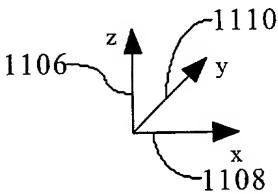
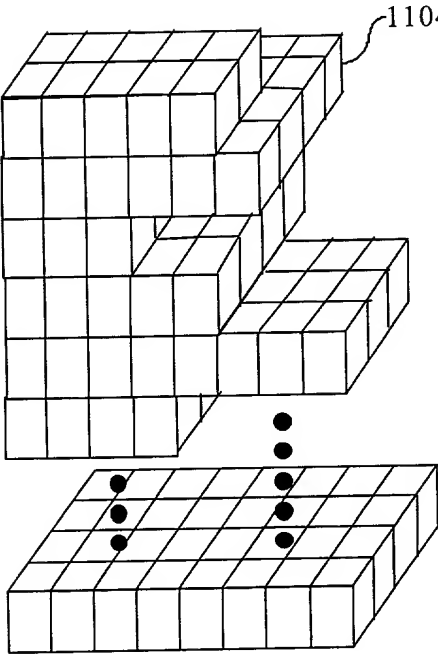
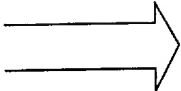


FIG 11

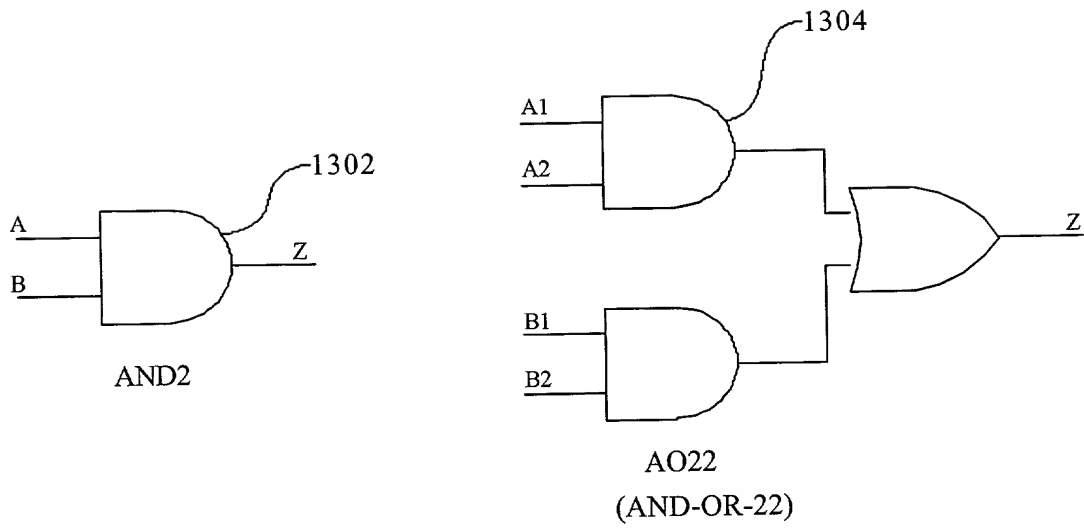
1200

| CHAR<br>POSITION<br>(0 OFFSET) | CHAR<br>VALUE | Correlation<br>Set<br>(x') | Entry<br>Position<br>(y') | Slot<br>Offset<br>(x'') |
|--------------------------------|---------------|----------------------------|---------------------------|-------------------------|
| 0                              | 1             | N/A                        | N/A                       | N/A                     |
| 1                              | 4             | 1                          | 5th                       | 1st                     |
| 2                              | X             | 1                          | 60th                      | 2nd                     |
| 3                              | a             | 1                          | 11th                      | 3rd                     |
| 4                              | m             | 1                          | 26th                      | 4th                     |
| 5                              | p             | 1                          | 29th                      | 5th                     |
| 6                              | l             | 1                          | 25th                      | 6th                     |

*FIG 12*

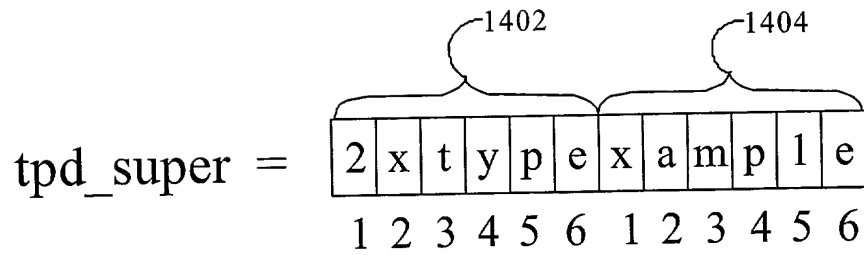
202010005US1

1300



*FIG 13*

1400

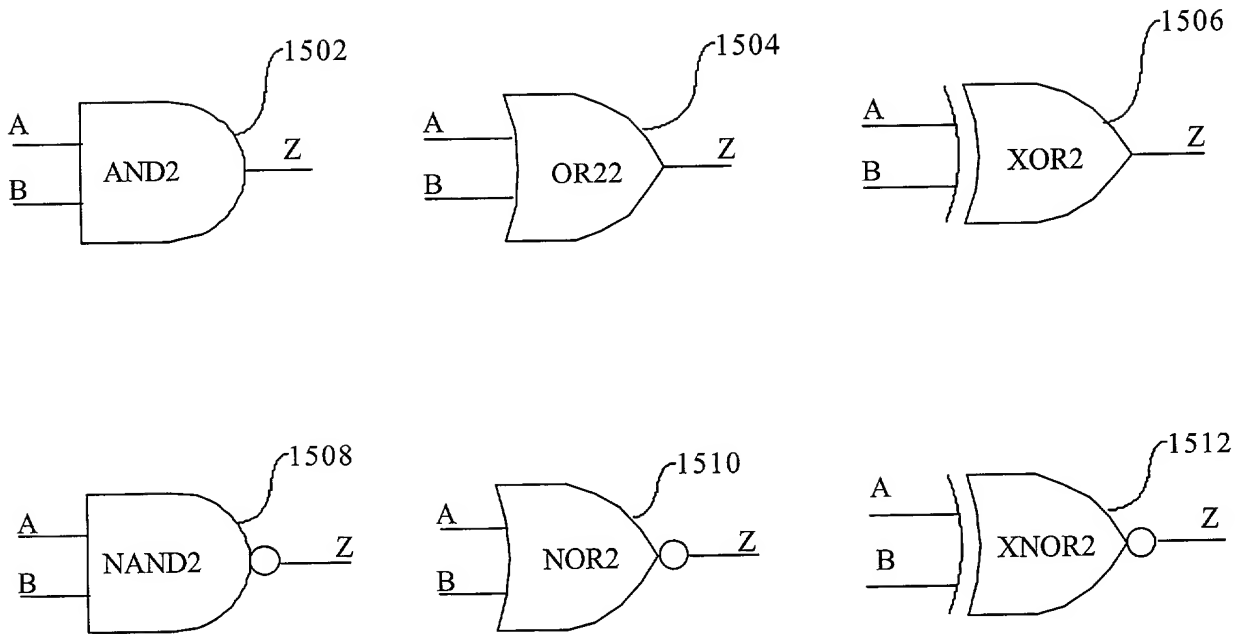


Correlation  
set expanded  
for each generic

- 1 → tpd\_A
- 2 → tpd\_B
- 3 → tipd\_A
- 4 → tipd\_B
- 5 → tpd\_A\_Z
- 6 → tpd\_B\_Z

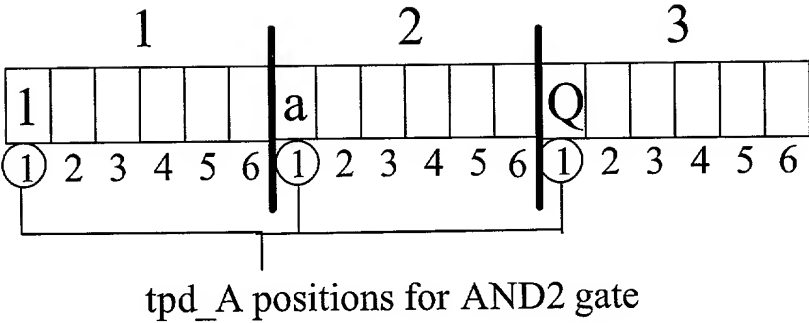
*FIG 14*

1500



*FIG 15*

1600

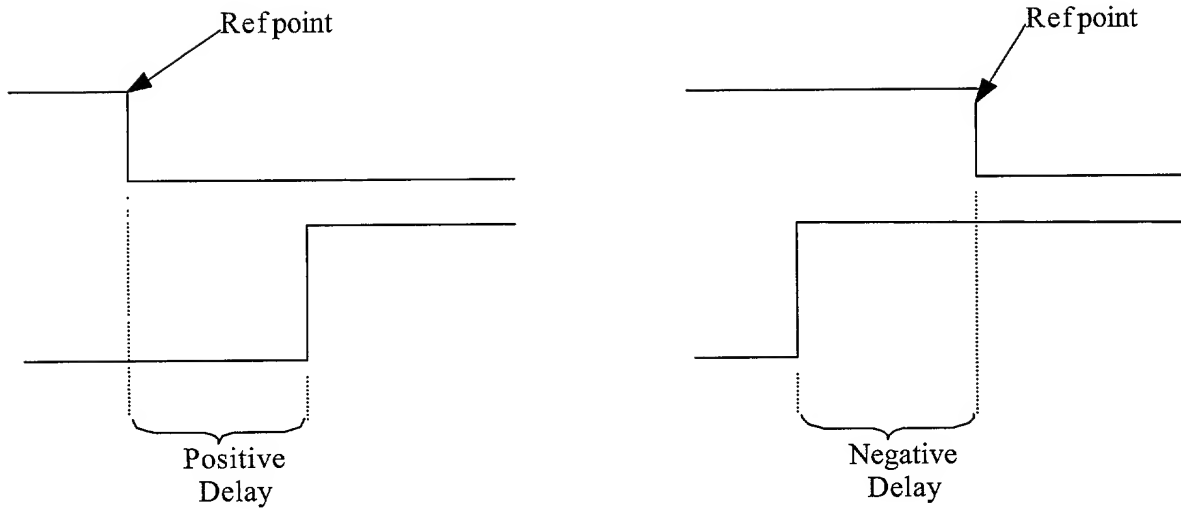


Encode as:

| DELAY       | tpd A |   |   |
|-------------|-------|---|---|
| DELAY       | 1     | 2 | 3 |
| -0.500 ns   | 0     | 0 | 0 |
| -0.499 ns   | 0     | 0 | 1 |
| +237.826 ns | Z     | Z | Y |
| +237.827 ns | Z     | Z | Z |

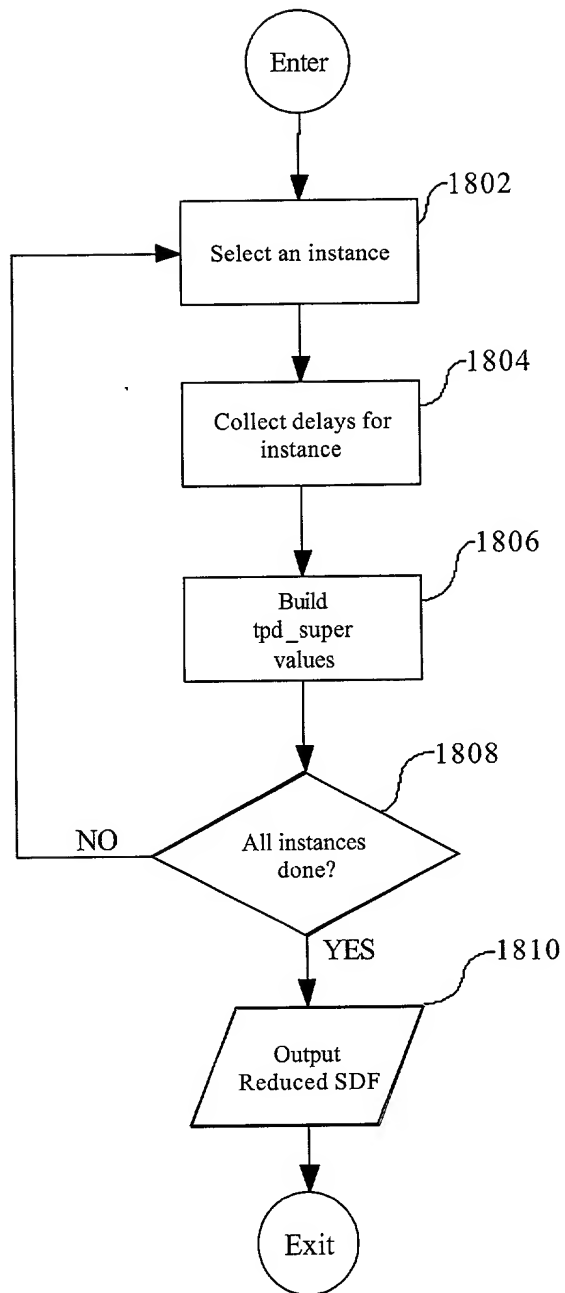
FIG 16

1700



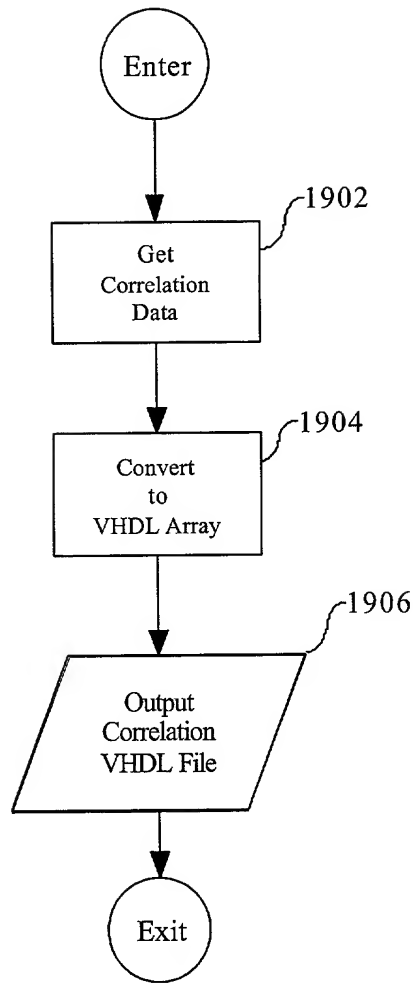
*FIG 17*

406



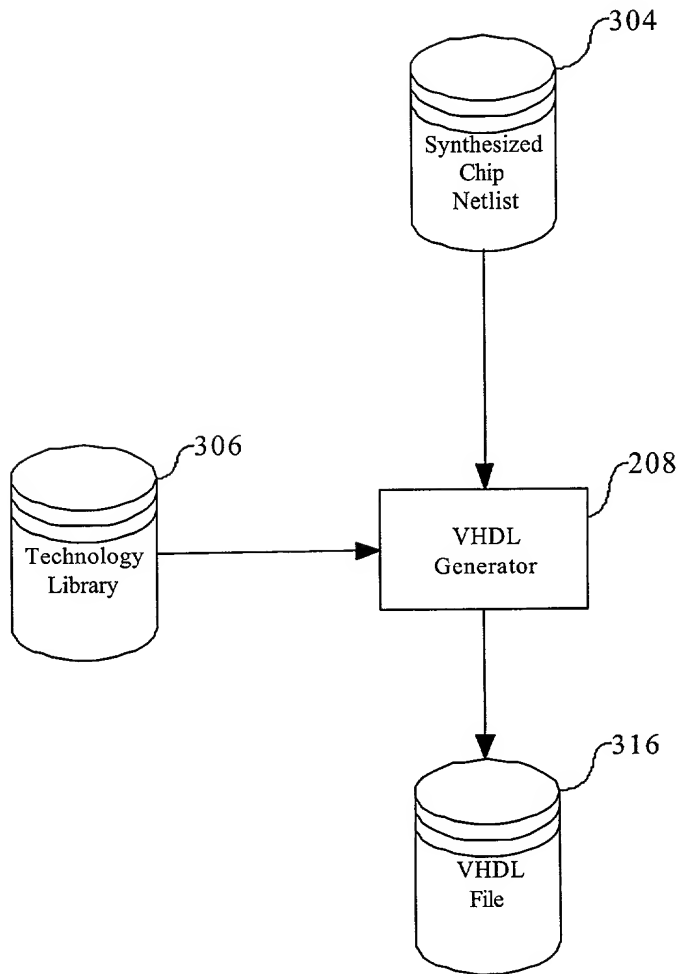
*FIG 18*

408



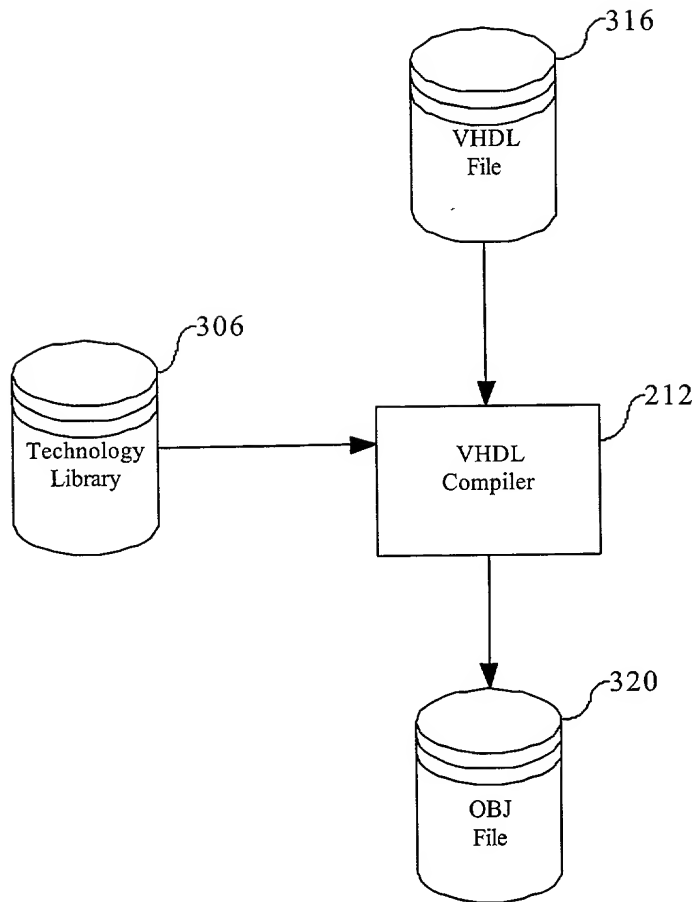
*FIG 19*

412



*FIG 20*

418



*FIG 21*

420

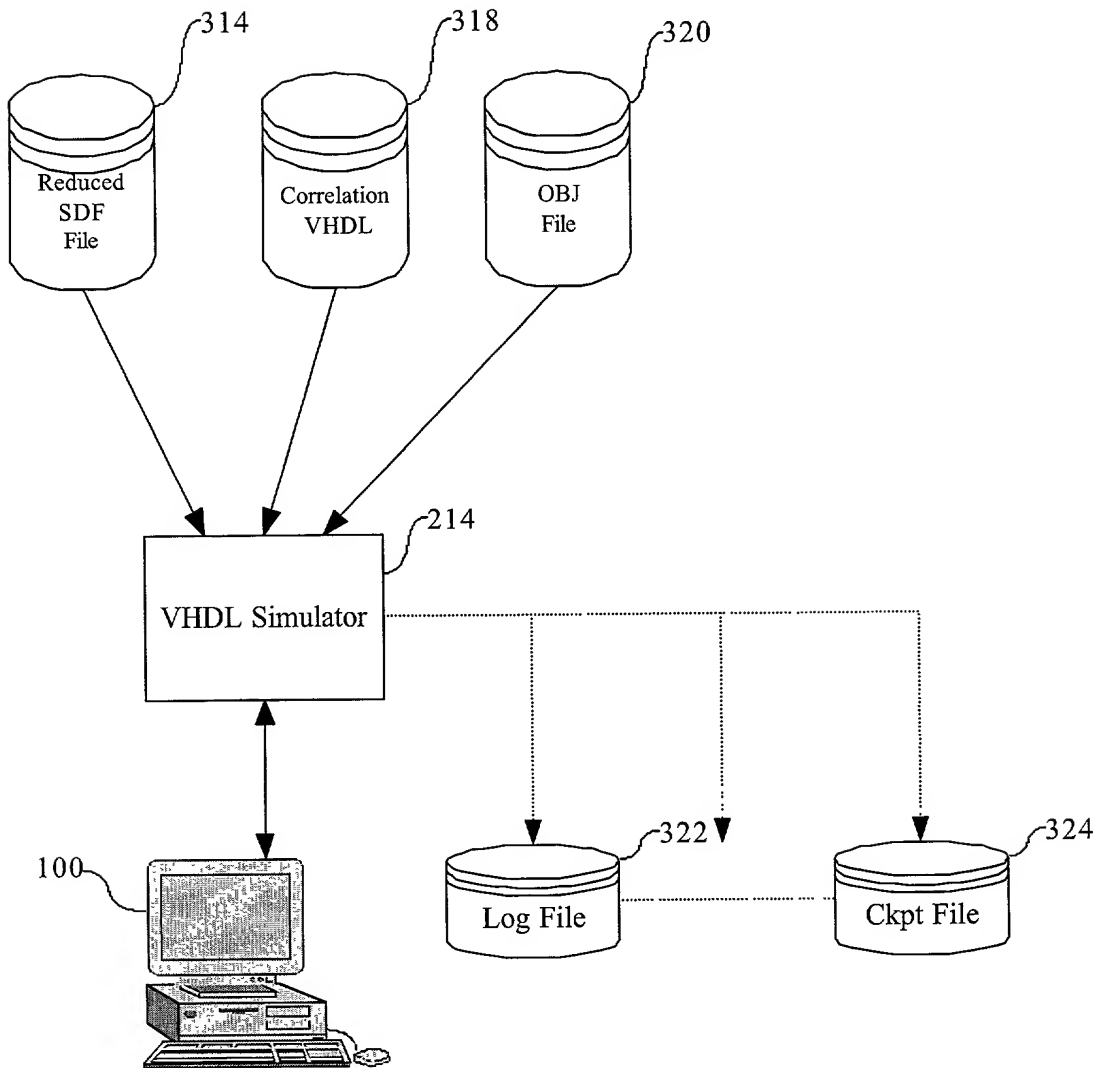


FIG 22